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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,961	09/26/2003	Glenn J. Leedy	ELM-2 CONT. 4	9439

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FISH & NEAVE IP GROUP
ROPES & GRAY LLP
1211 AVENUE OF THE AMERICAS
NEW YORK, NY 10036-8704

EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
07/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,961	LEEDY, GLENN J.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *88-128* is/are pending in the application.

4a) Of the above claim(s) *89-94,96-105 and 115* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *88,95,106-109,111-114,116-123 and 125-128* is/are rejected.

7)☒ Claim(s) *110 and 124* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed April 27, 2007.

Information Disclosure Statement

2. The information disclosure statement filed 4/27/07 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 88, 95 and 116-119 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Hubner (U.S. Patent No. 5,902,118).

In regards to claim 88, Hubner discloses the following:

a) a first substrate (26) comprising a first surface having interconnect contacts (210) formed thereon (For Example: See Figure 2); and

b) a second substrate (21) comprising a first surface having interconnect contacts (25) formed thereon, the first surface of the second substrate being bonded by thermal diffusion to the first substrate to form conductive paths between the interconnect contacts of the first surfaces of the first and second substrates, wherein the second substrate is a thinned substrate having circuitry formed thereon (For Example: See Figure 2 and Column 5 Lines 12-60) (Note: The bonding layer is heated and when metals heat (i.e. thermal) they diffuse, hence thermal diffusion bonding).

Finally, the following limitation makes it a product by process claim: a) "by thermal diffusion." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claims 95 and 119, Hubner discloses the following:

a) at least one additional thinned substrate (214) having circuitry formed thereon (For Example: See Figure 4, Column 6 Lines 3-14);

b) a first of said at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent thinned substrates (For Example: See Figure 4); and

c) conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrates and also between each additional thinned substrate and at least one of said substrates of the integrated structure (For Example: See Figure 4).

In regards to claim 116, Hubner discloses the following:

a) a first substrate (26) having topside and bottomside surfaces, the topside surface of the first substrate having interconnect contacts formed thereon (For Example: See Figure 4);

b) a second substrate (21) having topside and bottomside surfaces, the bottomside surface of the second substrate having interconnect contacts formed thereon and being bonded by thermal diffusion to the topside surface of the first substrate (For Example: See Figure 4) (Note: The bonding layer is heated and when metals heat (i.e. thermal) they diffuse, hence thermal diffusion bonding); and

c) conductive paths formed between the interconnect contacts on the topside of the first substrate and the bottomside of the second substrate, the conductive paths providing electrical connections between the first substrate and the second substrate, wherein the second substrate is a thinned substrate having circuitry formed thereon (For Example: See Figure 4).

Finally, the following limitation makes it a product by process claim: a) "by thermal diffusion." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in

"product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 117, Hubner discloses the following:

a) selected ones of said interconnect contacts on said topside surface are in electrical contact with selected ones of the interconnect contacts on said bottomside of said second substrate so as to form said electrical connection (For Example: See Figure 4).

In regards to claim 118, Hubner discloses the following:

a) a first substrate (For Example: See Figure 4);

b) a second substrate wherein the first substrate has a first surface bonded by thermal compression to a first surface of the second substrate and wherein the first and second substrate have second surfaces opposite to said first surfaces (For Example: See Figure 4) (Note: The bonding layer is heated and when metals heat (i.e. thermal) they diffuse, hence thermal diffusion bonding/compression); and

c) conductive paths formed on the first surfaces of the first and second substrates, wherein the second substrate is a thinned substrate having circuitry formed thereon (For Example: See Figure 4).

Finally, the following limitation makes it a product by process claim: a) "by thermal compression." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA

1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

5. Claims 106-108, 111-114, 120-122 and 125-128 are rejected under 35 U.S.C. 103(a) as obvious over Hubner (U.S. Patent No. 5,902,118) in view of Faris (U.S. Patent No. 5,786,629) and Sakui et al. (U.S. Patent No. 5,615,163).

In regards to claims 106 and 120, Hubner fails to disclose the following:

a) at least one controller substrate having logic circuitry formed thereon and at least one memory substrate having memory circuitry formed thereon.

However, Faris discloses at least one controller substrate having logic circuitry formed thereon and at least one memory substrate having memory circuitry formed thereon (For Example: See Column 3 Lines 60-63, Column 7 Lines 8-13 and Column 12 Lines 5-10). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hubner to include at least one controller substrate having logic circuitry formed thereon and at least one memory substrate having memory circuitry formed thereon as disclosed in Faris because it aids in providing parallel data processors (For Example: See Column 3 Lines 60-63).

Additionally, since Hubner and Faris are both from the same field of endeavor, the purpose disclosed by Faris would have been recognized in the pertinent art of Hubner.

b) a plurality of data lines and a plurality of gate lines on each memory substrate and an array of memory cells on each memory substrate each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines.

However, Sakui et al. ("Sakui") discloses a plurality of data lines and a plurality of gate lines on each memory substrate and an array of memory cells on each memory substrate wherein memory cells store a data value and have circuitry that couple the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines (For Example: See Figure 10, Column 5 Lines 20-67 and Column 6 Lines 1-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hubner to include a plurality of data lines and a plurality of gate lines on each memory substrate and an array of memory cells on each memory substrate wherein memory cells store a data value and have circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines as disclosed in Sakui because it aids in providing a means for saving the efficiency of a defective bit (For Example: See Column 5 Lines 11-18 and Column 6 Lines 40-63).

Additionally, since Hubner and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Hubner.

c) a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment.

However, Sakui discloses a gate line selection circuit (22, 23, 24 and 22') that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hubner to include a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Hubner and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Hubner.

d) controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

However, Sakui discloses controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hubner to include controller

substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Hubner and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Hubner.

In regards to claims 107 and 121, Hubner fails to disclose the following:

a) the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

However, Sakui discloses that the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hubner to include that the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Hubner and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Hubner.

In regards to claims 108 and 122, Hubner fails to disclose the following:

a) programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

However, Sakui discloses programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hubner to include programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Hubner and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Hubner.

In regards to claims 111 and 125, Hubner fails to disclose the following:

a) logic circuitry of the at least one controller substrate performs functional testing of a substantial portion of the array of memory cells.

However, Sakui discloses logic circuitry of the at least one controller substrate that performs functional testing of a substantial portion of the array of memory cells (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hubner to include logic circuitry of the at least one controller substrate that performs functional testing

of a substantial portion of the array of memory cells as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Hubner and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Hubner.

In regards to claims 112 and 126, Hubner fails to disclose the following:

a) the controller substrate logic is further configured to: prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line.

However, Sakui discloses that the controller substrate logic is further configured to prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hubner to include that the controller substrate logic is further configured to prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Hubner and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Hubner.

In regards to claims 113 and 127, Hubner fails to disclose the following:

a) the controller substrate logic is further configured to prevent the use of at least one defective gate line.

However, Sakui discloses that the controller substrate logic is further configured to prevent the use of at least one defective gate line (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hubner to include that the controller substrate logic is further configured to prevent the use of at least one defective gate line as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Hubner and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Hubner.

In regards to claims 114 and 128, Hubner fails to disclose the following:

a) the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate.

However, Sakui discloses that the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hubner to include that the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Hubner and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Hubner.

6. Claims 109 and 123 are rejected under 35 U.S.C. 103(a) as obvious over Hubner (U.S. Patent No. 5,902,118) in view of Faris (U.S. Patent No. 5,786,629), Sakui et al. (U.S. Patent No. 5,615,163) and Daberko (U.S. Patent No. 5,787,445).

In regards to claims 109 and 123, Hubner fails to disclose the following:

a) the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell.

However, Daberko discloses that the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell (For Example: See Abstract, Column 3 Lines 66 and 67, Column 4 Lines 1-11, Column 5 Lines 63-67 and Column 6 Lines 1-11). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Daberko to include that an array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell as disclosed in Daberko because it aids in providing direct manipulation of data segments (For Example: See Column 3 Lines 60-64).

Additionally, since Hubner and Daberko are both from the same field of endeavor, the purpose disclosed by Daberko would have been recognized in the pertinent art of Hubner.

Allowable Subject Matter

7. Claims 110 and 124 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed 4/27/07 have been fully considered but they are not persuasive. Applicant argues that "a solder bond, such as that described by Hubner is not a thermal diffusion bond. Thermal diffusion bonding or thermal compression bonding produces a bond that has a substantially different structure than a solder bond." MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted). The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product." *In re Garnero*, 412 F.2d 276, 279. Therefore, the Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature than when a product is claimed in the conventional fashion. See In re Fessmann, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale

tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. See In re Marosi, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir.1983). Arguments are not evidence. Applicant needs to present evidence establishing an unobvious difference between the claimed product and the prior art product.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization

where this application or proceeding is assigned is 571-273-8300 for regular and after final communications.

ML
July 11, 2007

MONICA LEWIS
PRIMARY PATENT EXAMINER